FIG. **10**B is a graph showing information that is generated by and/or helpful in understanding the thirteenth embodiment semiconductor structure;

FIG. **11**A is a cross-sectional view of a fourteenth embodiment semiconductor structure according to the present invention;

FIG. **11**B is an electrical schematic of the fourteenth embodiment semiconductor structure;

FIG. **11**C is a graph showing information that is generated by and/or helpful in understanding the fourteenth embodiment semiconductor structure;

FIG. **12**A is a cross-sectional view of a fifteenth embodiment semiconductor structure according to the present invention;

FIG. **12**B is a cross-sectional view of a sixteenth embodiment semiconductor structure according to the present invention;

FIG. **12**C is a graph showing information that is generated by and/or helpful in understanding the fifteenth embodiment semiconductor structure; and

FIG. **12**D is a cross-sectional view of a seventeenth embodiment semiconductor structure according to the present invention.

DETAILED DESCRIPTION

Some embodiments of the present invention recognize: (i) that thin-film heterojunction field-effect transistor (HJFET) devices with c-Si channels and PECVD contact regions (a) can be processed on thin single-crystalline substrates using the mainstream large area deposition techniques used for non-crystalline materials (for example, amorphous Si) and/or (b) provide substantially higher performance than a-Si:H TFTs; (ii) that the c-Si channel of such HJFET devices can be also formed by recrystallized polycrystalline silicon (poly-Si) using various known techniques; (iii) that the gate region of such an HJFET may be comprised of a-Si:H structurally similar to the emitter of heterojunction solar cells with intrinsic thin layers; (iv) that the source and drain regions may be comprised of hydrogenated crystalline silicon (c-Si:H) grown epitaxially on c-Si using the same PECVD reactor as a-Si:H at temperatures close to 200° C. (well below 250° C.); and/or (v) that this approach allows the use of existing a-Si:H deposition infrastructure for the fabrication of such HJFET devices.

In some embodiments of the present invention, a blocking structure is incorporated into the gate stack of a junction field-effect transistor (JFET) device to substantially suppress the gate current when the gate junction is forward-biased. As a result, normally-OFF JFET devices with MOSFET-like characteristics are obtained. The JFET devices are comprised of gate, source and drain regions and may be formed, for example, by plasma-enhanced chemical vapor deposition (PECVD) on thin-film crystalline Si (c-Si) substrates at temperatures below 200° C. (well below 250° C.). The HJFET devices can be integrated with MOSFET devices fabricated on the same c-Si substrates to form complementary circuits.

Some embodiments of the present invention recognize one or more of the following facts, potential problems and/or potential areas for improvement with respect to the current state of the art: (i) a JFET or HJFET has a simpler structure than a MOSFET; (ii) advantages of the HJFET structure over the more commonly-used metal-oxide-semiconductor field-effect transistor (MOSFET) include the established stability of the a-Si:H/c-Si heterojunction as well as lower operating voltages due to the elimination of the low-temperature gate dielectric; (iii) despite these advantages, HJFET devices are prone to high gate leakages if the gate heterojunction is forward-biased; and/or (iv) this shortcoming limits the practical application of HJFET devices to normally-ON transistors.

As a result, some embodiments of the present invention may include one or more of the following features, characteristics and/or advantages: (i) a JFET and/or HJFET structure with an improved gate stack to block gate current at forward bias; (ii) normally-OFF devices which are not possible with conventional JFET or known HJFET structures; (iii) use of the same deposition techniques compatible with mainstream large-area processing for producing the devices of (i) and/or (ii); (iv) usage in the pixel circuits of active-matrix organic light-emitting diode (AMOLED) backplanes; and/or (v) the formation of complementary circuits through interconnection of the devices of (i) and/or (ii) with MOSFET devices fabricated on the same substrate.

Some embodiments of the present invention recognize: (i) that the features, characteristics and/or advantages described above may be of value for integrating AMOLED backplane driver/control circuitry on the same substrate as the HJFET backplane; (ii) they the features, characteristics and/or advantages described above may be of value for realizing complementary circuits for other applications in large-area electronics, such as logic and memory, provided that sufficiently reliable MOSFET devices are available; (iii) that reliability requirements for such applications are generally less stringent than those for the driver transistor in an AMOLED pixel, which is operated in direct current (DC) (that is, with a 100% duty cycle); (iv) that conventional complementary circuits with p-channel and n-channel MOSFETs on silicon-on-glass (SiOG) substrates require process temperatures of up to 600° C. for the activation of the p^+ and n^+ implanted source and drain regions; (v) that channel implantation is desired for adjusting the threshold voltage and reducing the sensitivity of the threshold voltage to parasitic fixed and/or trapped charge associated with the insulating substrate (for example, buried oxide (BOX) or glass); (vi) that high activation temperatures such as in (iv) preclude the use of a wide range of low-cost and flexible substrates; and/or (vii) that in contrast, some embodiments of the present invention require only one type of substrate doping, thereby eliminating the need for further substrate doping after substrate preparation.

Some embodiments of the present invention may include a complementary circuit scheme wherein the combination of an n-channel HJFET and a p-channel MOSFET includes an n-channel HJFET that provides a higher drive current than a p-channel HJFET (due to the higher mobility of electrons than holes) as well as a p-channel MOSFET that is far less sensitive to floating-body effects such as early break-down/kink effect than an n-channel MOSFET, and/or wherein the HJFET devices are expected to be immune to floating body effects regardless of the substrate type (because the parasitic bipolar transistor inherent to the MOSFET structure does not exist in the HJFET structure).

Some embodiments of the present invention recognize: (i) that normally-OFF HJFET devices can be created by incorporating an a-Si:H blocking stack in the gate heterojunction to substantially suppress the gate leakage at forward-bias conditions; and/or (ii) that such HJFET devices can be integrated with MOSFETs on the same c-Si substrate to achieve complementary circuits.

Shown in FIGS. **1**A and **1**B are schematic cross-sectional views of HJFETs **100***a* and **100***b*, respectively, which are two variations on embodiments of the present invention.